Overview of Single Tile Processing System Goals, Specifications and Timeline

Bob Wagner

LAPPD Single Tile Facility Review

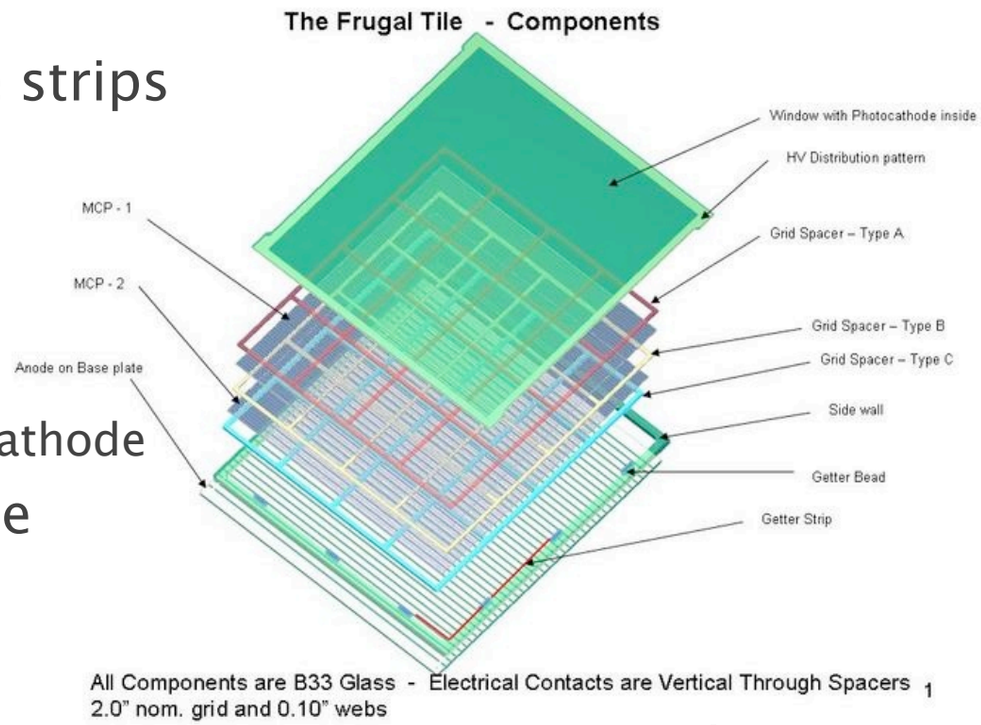
Friday 16 March 2012

Why a Single Tile Facility?

- Produce small numbers of single Large Area MCP Photodetectors
  - Characterization by LAPPD group (gain, timing, QE, aging,…
  - Distribute to HEP, Nuclear, Medical Imaging, Security community
- Provide platform for further development of LAPPD detector
  - Demonstrate new developments by incorporating them into test detectors
    - Improved Photocathodes
    - New ALD coatings
  - Produce alternative formats, e.g. 2”×2”, 33mm circular
- Maintain and utilize expertise and techniques built up over last 3 years
- Possible user facility for trying ideas of experimenters from universities, other national labs
  - Part of comprehensive photodetector R&D facility for Argonne including Photocathode Development Lab

Goals of Single Tile Processing System (STPS)

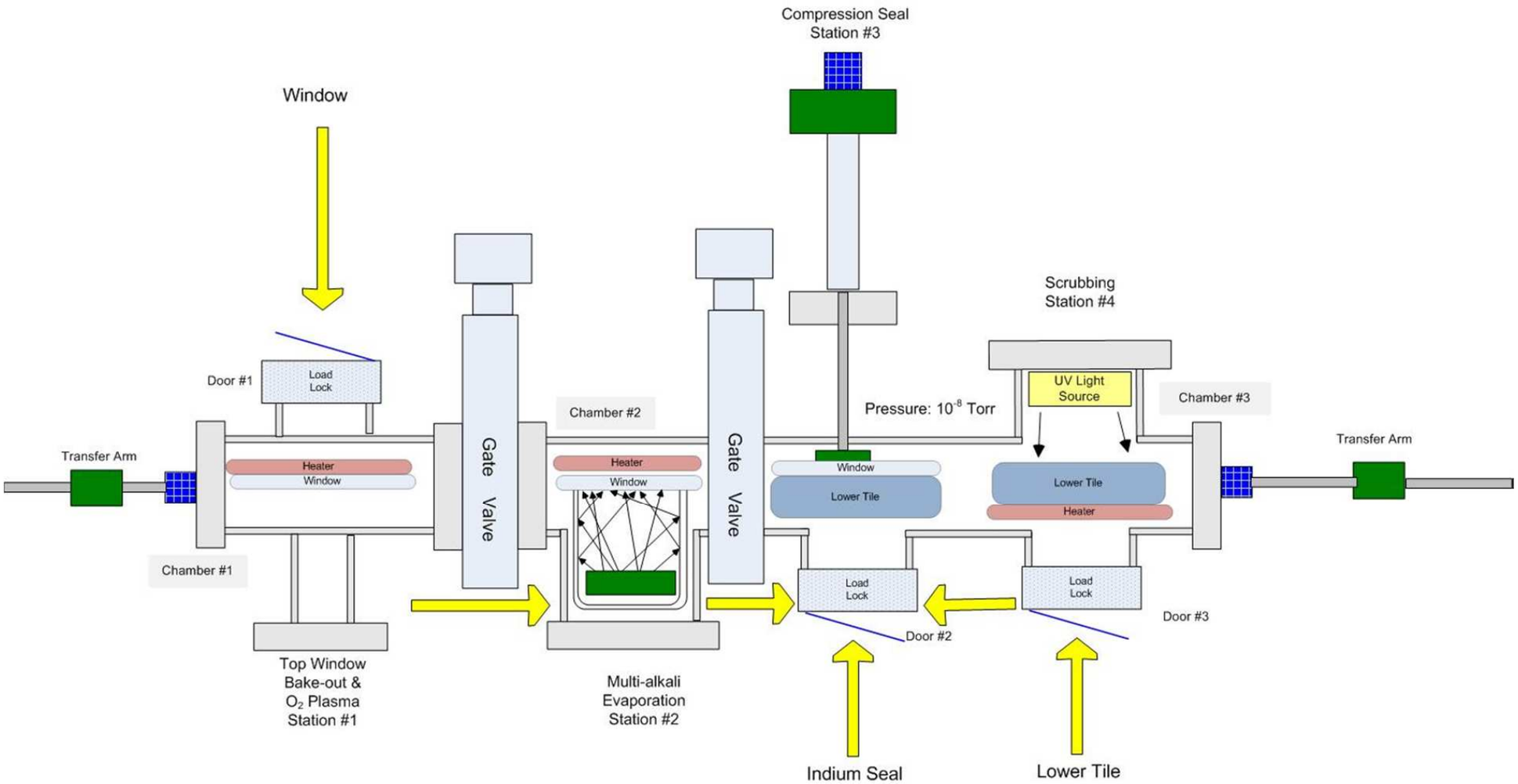
- Production of all borosilicate glass 8”×8” active area MCP sealed photodetector tiles
  - Bottom plate with silk-screened silver anode strips
  - ALD functionalized glass capillary MCP pair
  - Grid spacers for mechanical support and voltage distribution
    - ALD coated to target resistance
    - separate anode/MCP2, MCP2/MCP1, MCP1/photocathode
  - Top window with bialkali (K,Cs) photocathode
  - Getter material
  - Bottom plate frit-sealed to glass sidewall
  - Top window bonded to sidewall using thermopressure indium wire seal
- Production will be **one tile assembly** at a time
- Design to allow alternative formats and fabrications, e.g. 2”×2” MCP tile, new photocathode materials



Components/Specifications for Single Tile System

- Parts going into STPS
  - Tile base (anode bottom plate frit-sealed to sidewall) with MCP/grid spacer internal stack. Assembled in ALD lab clean enclosure??? Bring protected parts to STF Clean Enclosure and assemble???
    - Getters loaded into assembly
  - Top window
  - Indium wire seal pre-form
- Tile Base
  - 9mm sidewall. Wall thickness is 0.2” (5mm)
  - 8.66” × 9.02” anode plate with 30 silver anode strips
- 8” Microchannel Plates
  - Delivered to STPS electroded, functionalized, clean, and with minimal dust
  - Pair gain of 10^6–10^7
- Grid Spacers
  - 2mm thickness — top and interMCP spacer
  - ~2.6mm — bottom spacer (sized so internal stack in compression with top window)
  - Resistance determined by MCP resistance so as to provide ~1000V bias to each MCP
- Photocathode
  - 8” active area
  - QE goal is 25%
- Indium Top Seal
  - 2mm diameter indium wire
  - Pressure seal (crush wire) at ≤ 100˚C

Single Tile Process System



Top Window: Bake ➟ Photocathod Fab. ➟ Top Seal ⇐ Bake & Scrub :Tile Base

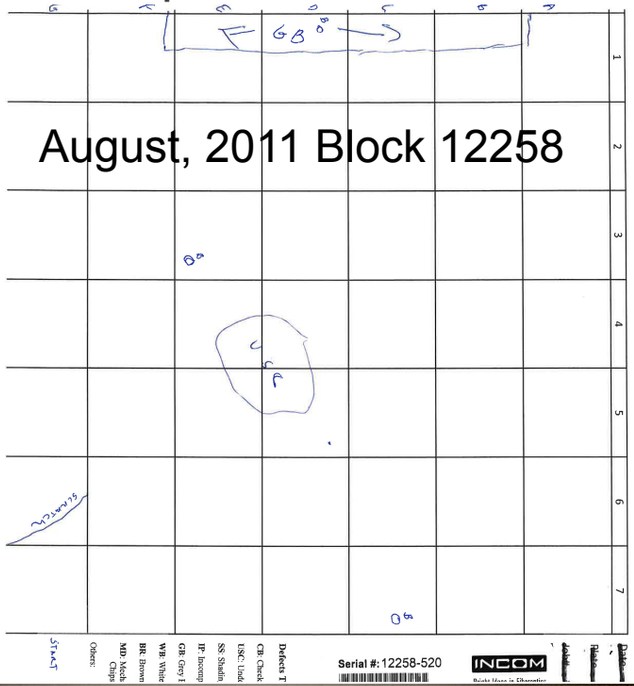
Will be covered in detail by Dean Walters

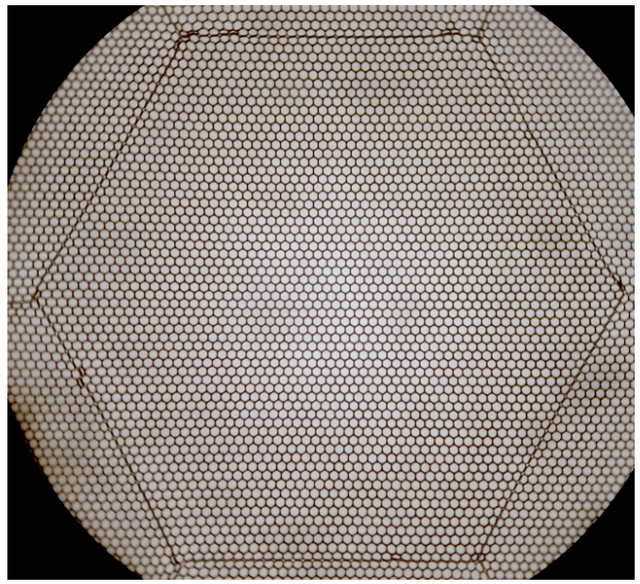
Personnel

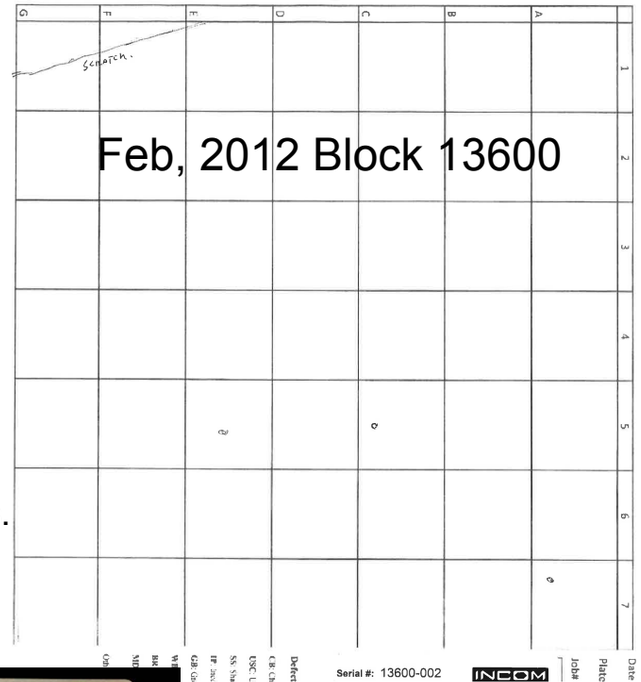
- Project Physicist — Bob Wagner
  - Responsible for planning, coordination and execution of STF
- Project Engineer — Dean Walters
  - Responsible for design of vacuum transfer system, pumps, heaters, gauges, valves, load-locks, manipulators, integration
- Single Tile Facility Manager — Jeff Williams
  - Oversee lab infrastructure installation
  - Construction & commissioning of STPS
  - Day-to-day operation of STPS
- Photocathode — Zikri Yusof
  - Development of photocathode: Burle tubes, 4"+ chalice, 8" tile photocathode
  - Transfer cathode subsystem in STS
  - Team includes Junqi Xie, Sasha Paramonov, Anatoly Ronzhin (Fermilab), Greg Sellberg (Fermilab)
- Top Seal — Dean Walters & Marc Kupfer
  - Development of 1", 4", 8" indium seals
  - Glass-to-glass, glass-to-aluminum, glass-to-nichrome
  - Implementation of existing press seal equipment into STS
- Scrubbing — Bob Wagner?, Dean Walters?, new hire?
  - Design of scrubbing subsystem
  - Components acquisition
  - Requirements of scrubbing
- Additional Personnel
  - Will require at least one technician working for construction of STPS
  - Henry Frisch (UC/Argonne), Karen Byrum, Marcel Demarteau
  - Senior scientist hire for photocathode development?, postdoctoral appointee?

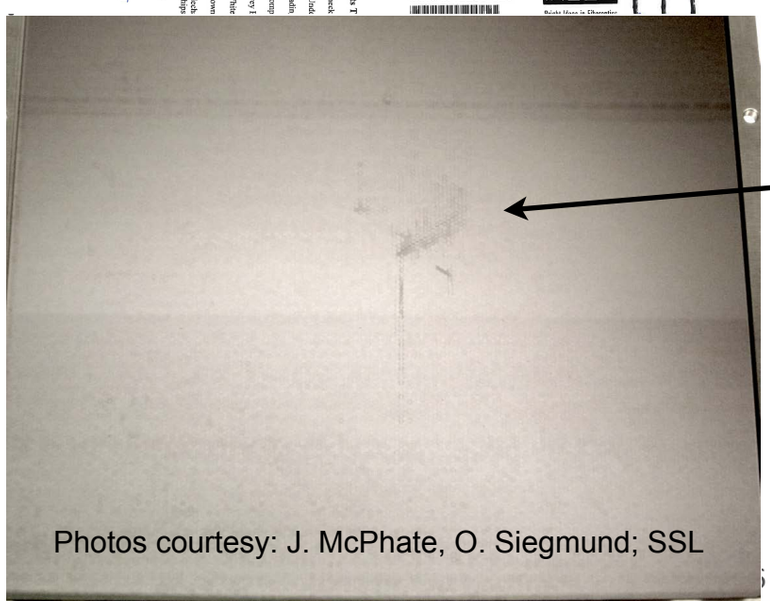
Steps to Success — Glass Capillary Arrays

- Microchannel Plate Development
  - Sole provider is Incom, Inc., Charlton, MA
  - Have developed materials & fabrication techniques for 33mm circular disks and 8”×8” plates over last 2.5+ years
  - Now producing consistently high quality disks and plates in quantity
  - Improvements in block fabrication, grinding, polishing, and cleaning are continuing





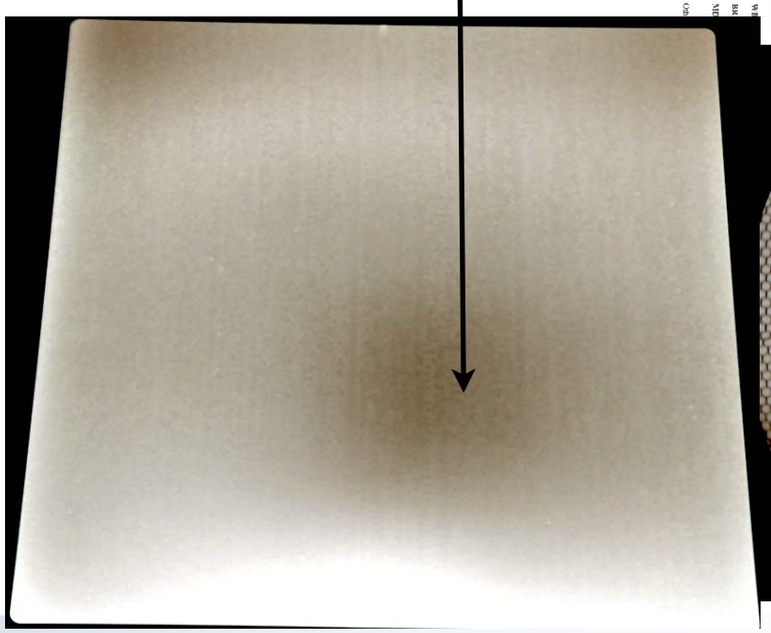


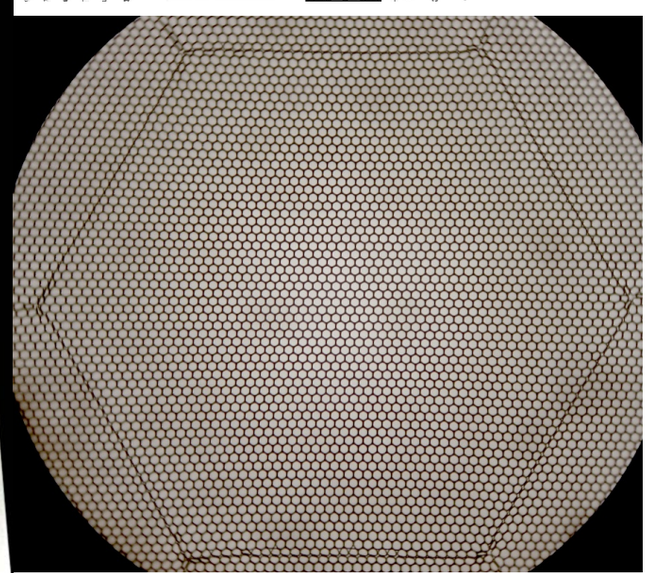


Smaller & distorted pore capillaries running through block: Hummingbird

Photos courtesy: J. McPhate, O. Siegmund; SSL

No gross defects. Artifact of photo





Steps to Success – ALD Functionalization

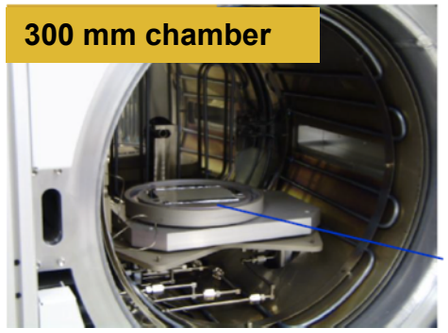
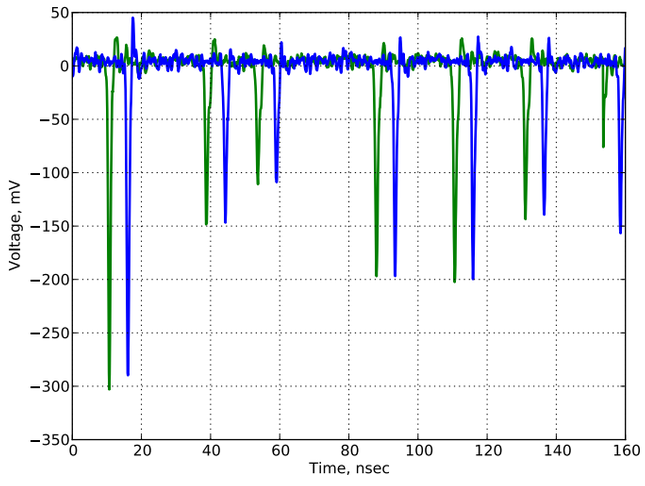
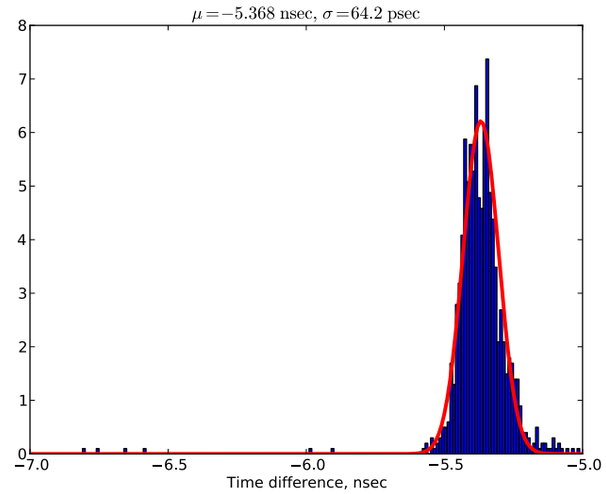


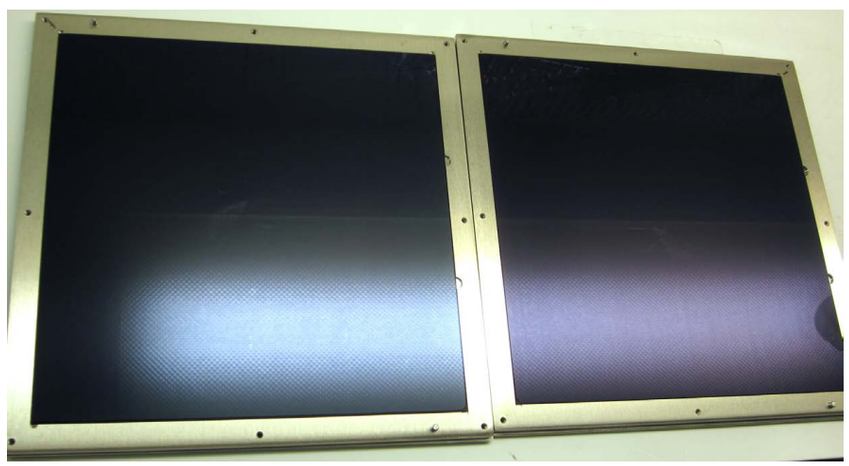
Photo courtesy: J. Elam, A. Mane

Beneq Commercial ALD
Reactor located in Bldg. 362





Signals by 8” MCP Pair, silver strip anode on glass, PSEC-4 ASIC readout

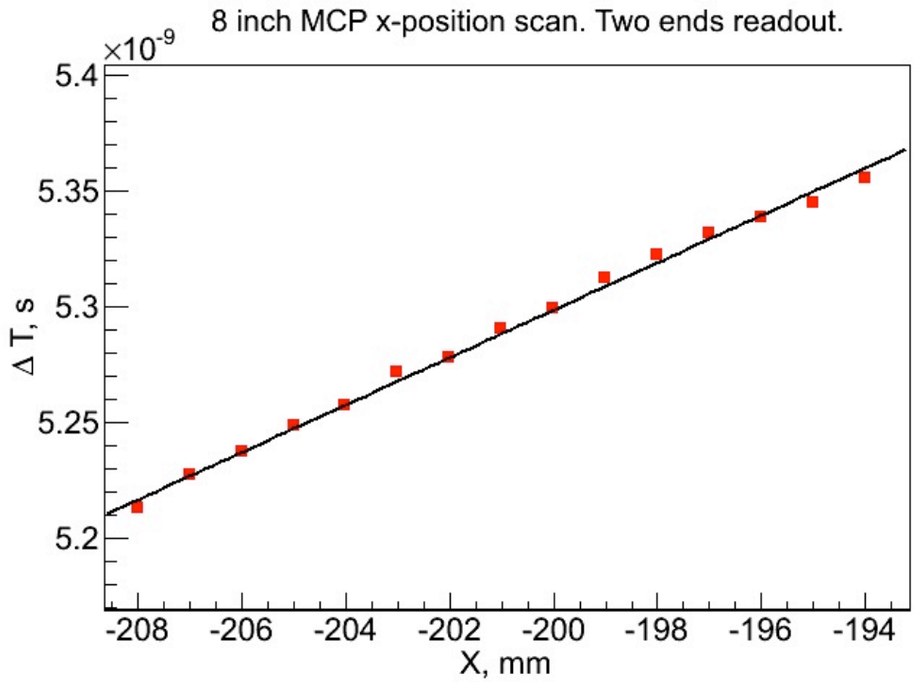


MCP 12258-536 - 5MΩ – top Is blue.

MCP 12258-544 - 8MΩ – Bottom Is purple

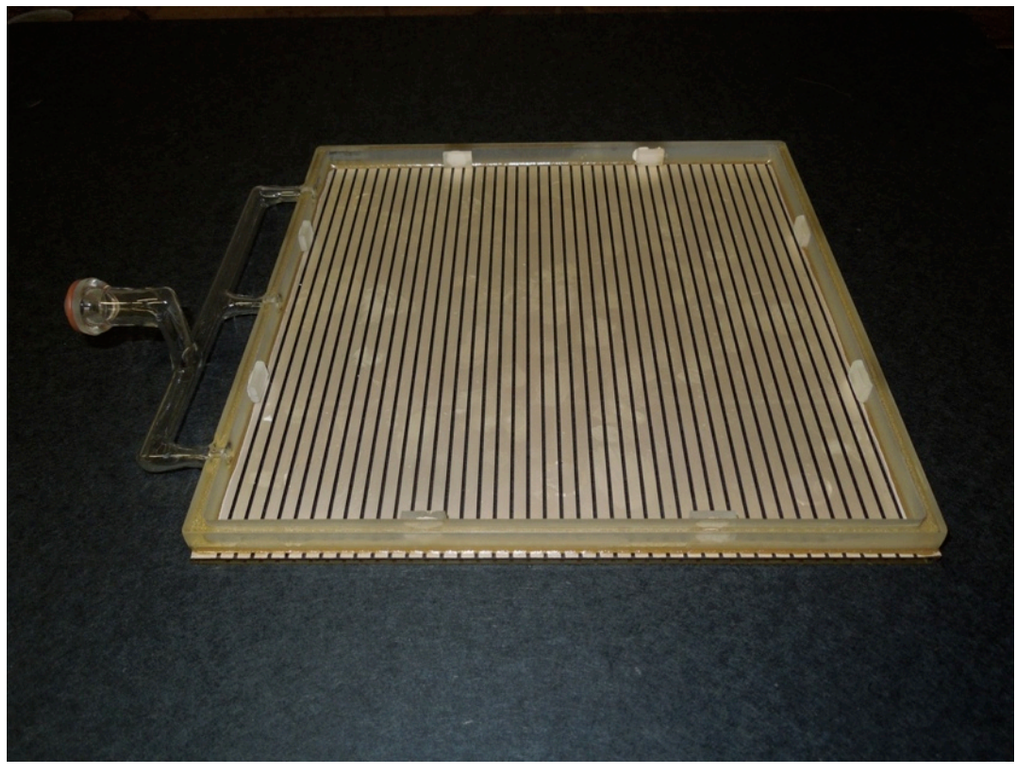
Photo courtesy: J. McPhate, O. Siegmund; SSL

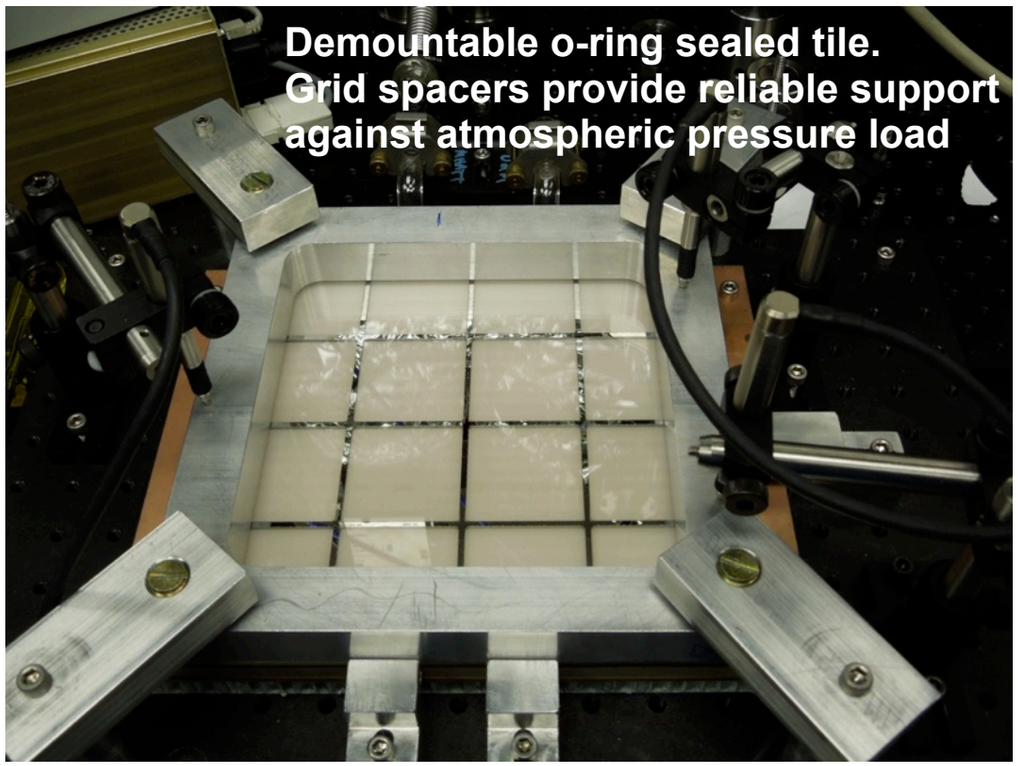
Coating uniformity greatly improved through understanding of reactor flow characteristics



Plots courtesy: A. Elagin, M. Wetstein, E. Oberla, R. Obaid, B. Adams, A. Vostrikov

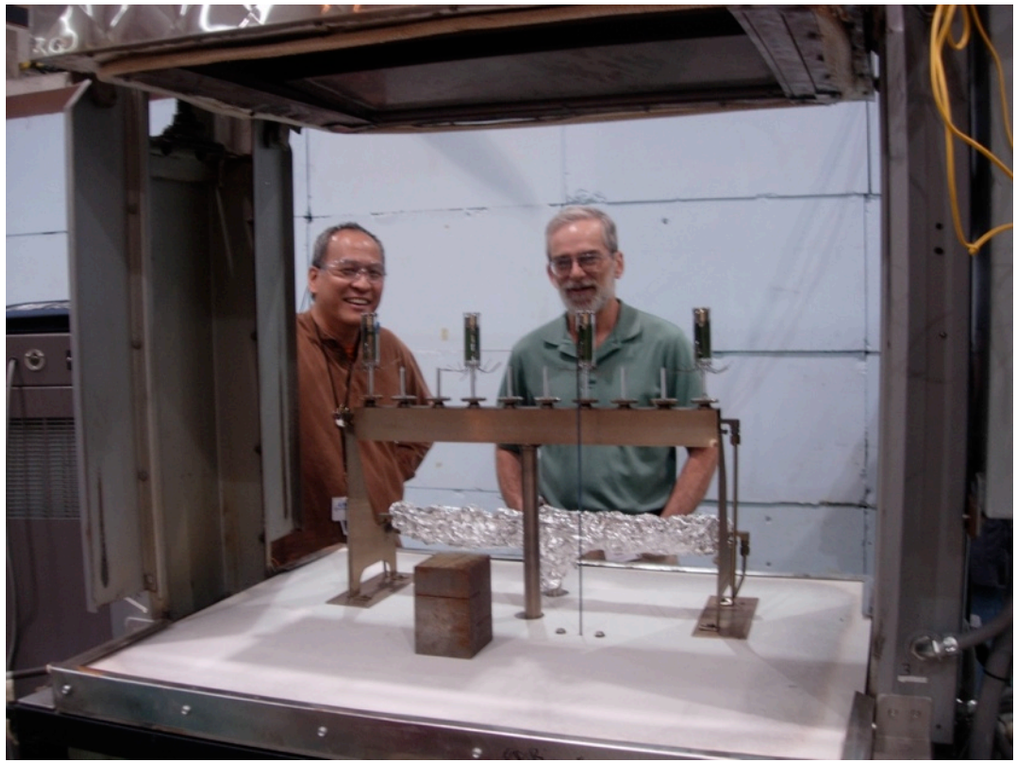
Steps to Success — Tile Bases, Grid Spacers, & Getter Holders

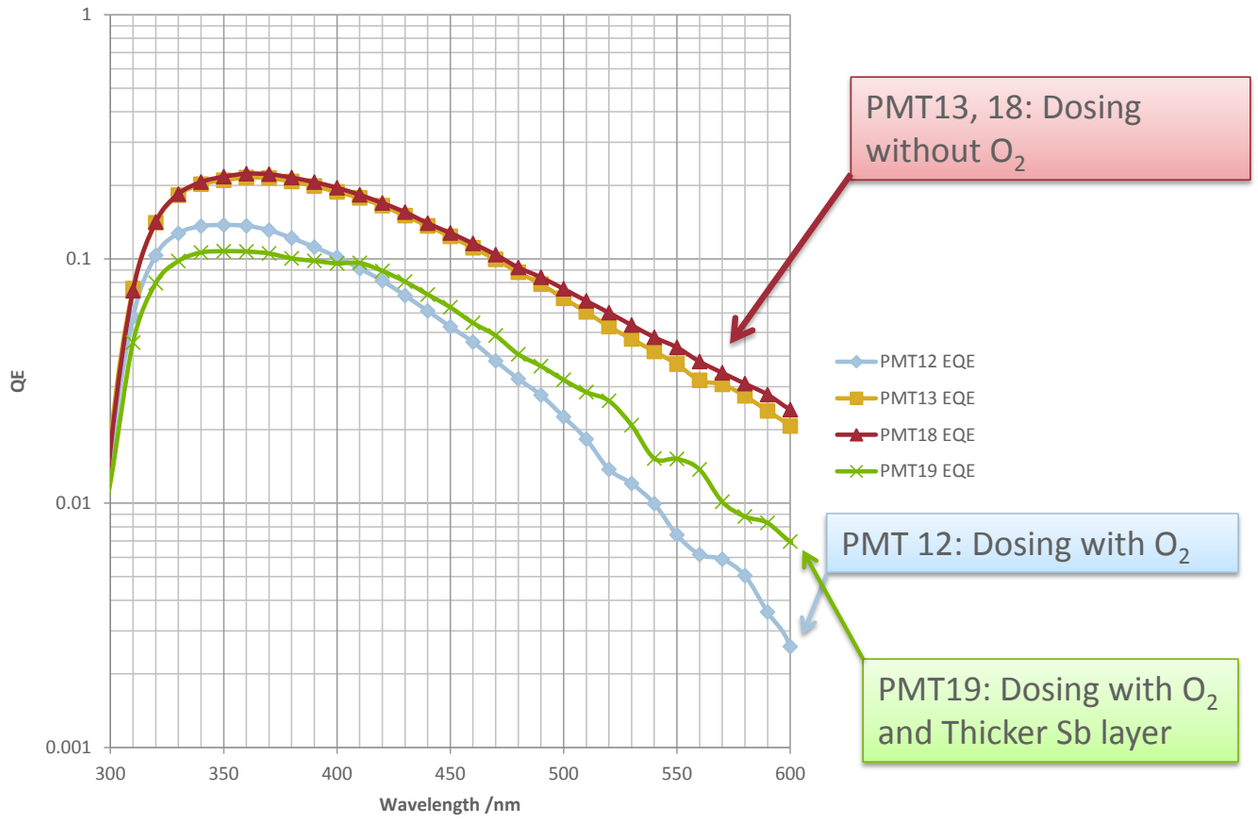




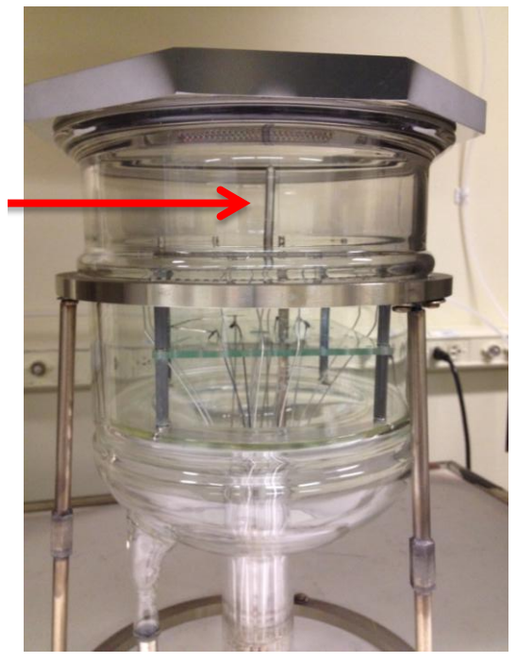
- Sidewall/Bottom plate hermetic bonding and attachments of getter holder/ spacers has been developed to a routine process
- Fabrication of precision thickness grid spacers and consistent sidewall height produce routine tile sealing without breakage

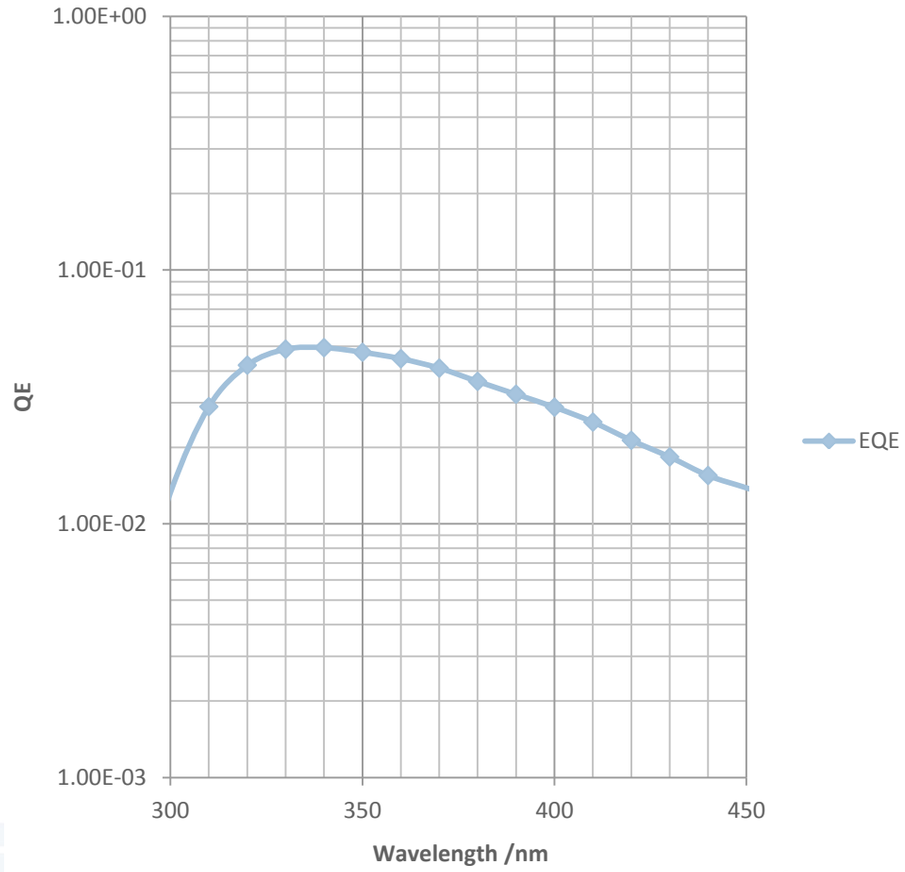
Steps to Success — Photocathode Development



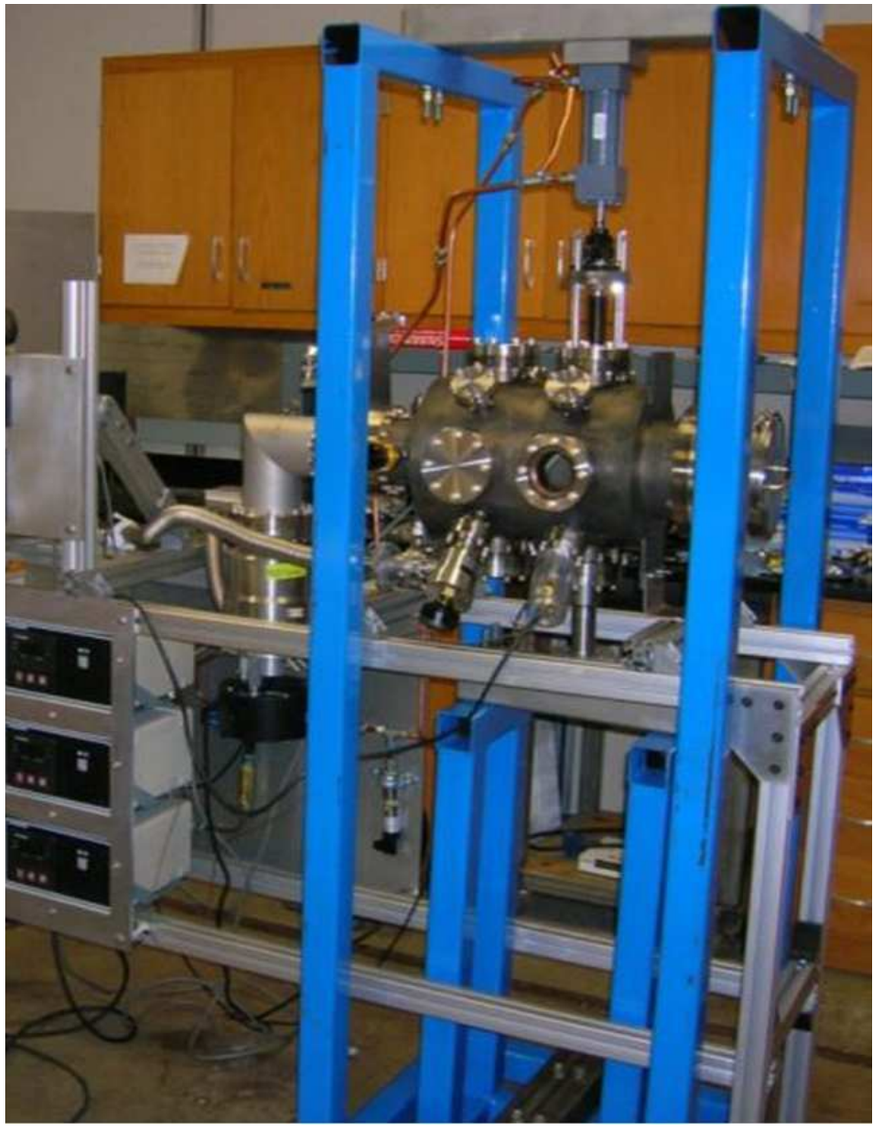


- PC deposition technique developed with Burle photodiode tubes (QE~15-23%)
- "Chalice" installed on Burle equipment for 4" PC development (1st attempt gives QE~5%)
- Chalice work continuing to address:
  - O2 plasma issues
  - Required amt. alkali material
  - QE improvement
  - Larger area coverage & uniformity

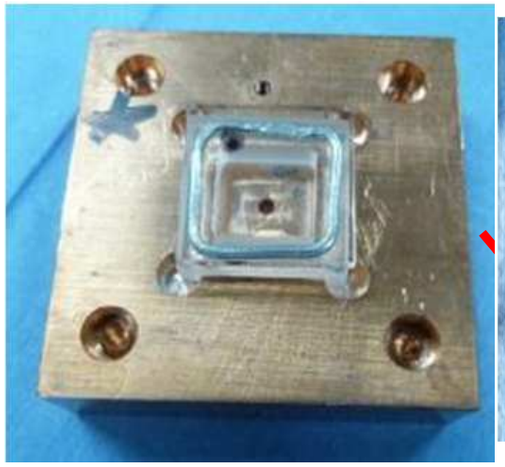




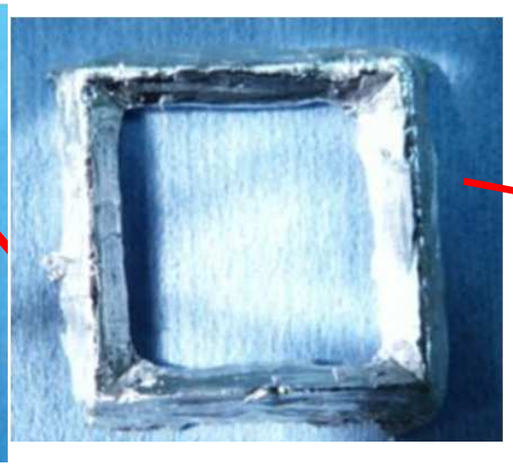
Steps to Success – Indium Thermopressure Top Seal

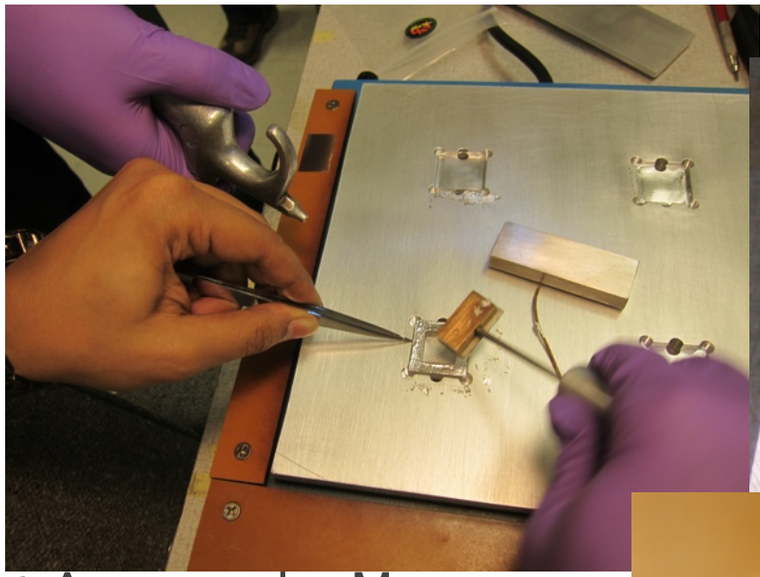


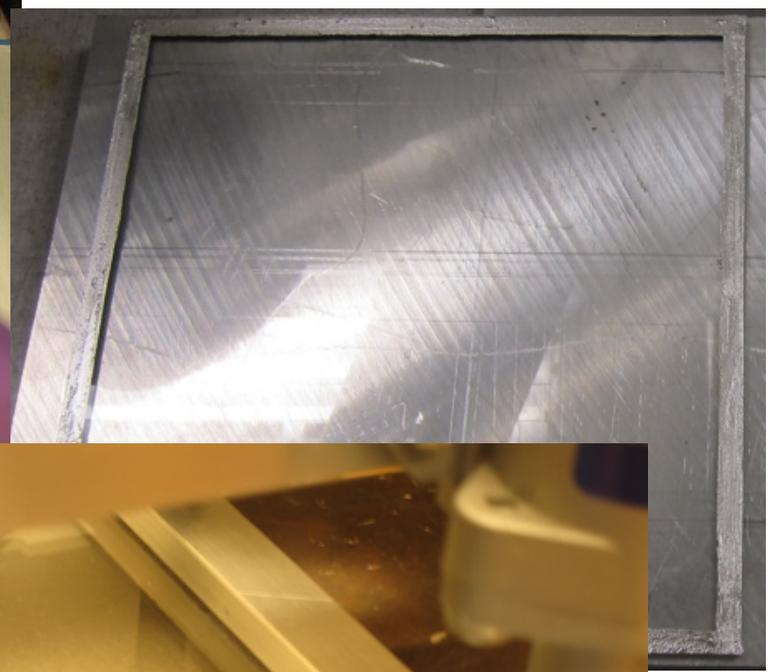
Single 2 mm

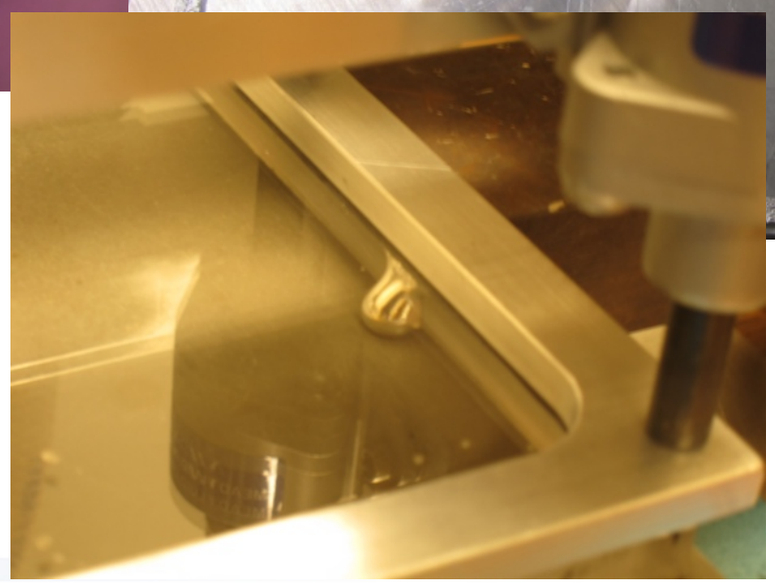


Cast Seal









- Vacuum indium sealing chamber built at Argonne by Marc Kupfer & Dean Walters
  - 1” & 4” glass sidewall/plate seals – routine success for 1”. First 4” seals now being made
  - Can be modified to do 8” sidewalls in air
- Tinned indium seal method at Univ. of Chicago
  - 1” seals routine. 8” sidewall sealing in progress

Timeline for STPS

	02-Apr-12	07-May-12	04-Jun-12	02-Jul-12	04-Aug-12	03-Sep-12	01-Oct-12	05-Nov-12	03-Dec-12	07-Jan-13	04-Feb-13	04-Mar-13	01-Apr-13	06-May-13	03-Jun-13	02-Jul-13	05-Aug-13	03-Sep-13	07-Oct-13	04-Nov-13	02-Dec-13	06-Jan-14	03-Feb-14	03-Mar-14	07-Apr-14
Single Tile Process System																								
1 Vacuum Transfer System																								
1.0 STPS Design																								
1.1 Chambers																								
1.2 Gate Valves																								
1.3 Gauges																								
1.4 Manipulators																								
1.5 Pumps																								
1.6 Heaters & Controls																								
1.7 Residual Gas Analyzer																								
1.8 Assembly																								
1.8.1 Support Stand																								
1.8.2 Chamber Assembly																								
1.8.3 Pump Installation																								
1.8.4 Leak Check																								
1.8.5 Bakeout																								
Estimated FTE	0.4	0.4	0.4	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	1.0	2.0	2.0	2.0	2.0	2.0	2.0	1.5	1.5			
2 Photocathode Subsystem																								
2.1 Chalice PC Development																								
2.2 STPS Cathode Vessel																								
2.2.1 Cathode Sys. Design																								
2.2.2 Vessel Fab.																								
2.2.3 Internals Constr.																								
2.2.4 Wiring																								
2.3 Optical Sys. Mods.																								
2.4 Plasma Etch Integration																								
2.5 Top Window Frame Holder																								
2.6 Initial Testing																								
2.6.1 Top Window Bake																								
2.6.2 Manipulation Tests																								
2.6.3 Cathode Test Shoots																								
2.7 First Production PC																								
Estimated FTE	1.5	1.5	2.0	2.0	2.0	2.0	0.5	1.5	1.7	1.7	1.0	1.0	1.2	1.5	1.2	0.5	0.5					1.0	1.0	1.5
3 Scrubbing & Baking Subsystem																								
3.1 Scrubber Design																								
3.2 Components Procurement																								
3.3 Scrubber Installation																								
3.4 Tile Base Bake Tests																								
3.5 Tile Base Manip. Tests																								
Estimated FTE							0.5	0.5	0.5	0.5	0.2	0.2	0.2	0.5	0.5	0.2								0.2
4 Top Seal Subsystem																								
4.1 1" & 4" Devel. Work																								
4.2 8" Work Existing Setup																								
4.2.1 Fixturing Fab.																								
4.2.2 Mold Fab.																								
4.2.3 8" Test Seals																								
4.3 Mod. Existing System																								
4.4 Installation in STPS																								
4.5 Initial Hydraulic Testing																								
4.6 Window Placement Testing																								
4.7 In Wire Placement Tests																								
4.8 Initial Seal Tests in Air																								
4.9 Initial Seal Tests in Vacuum																								
Estimated FTE	0.4	0.4	0.4	0.4	0.2	0.2	0.2	0.5								1.0	1.0	1.2	1.2			0.4	0.4	
5 Integration																								
5.1 Tile Fab - Scrap Parts																								
5.2 Tile Fab. - no PC																								
5.3 First Tile Fab. w/PC																								
Estimated FTE																							2.0	2.0
Total FTE	**2.5**	**2.5**	**3**	**2.9**	**2.7**	**2.7**	**1.7**	**3**	**2.7**	**2.7**	**1.7**	**1.7**	**2.4**	**4**	**3.7**	**3.7**	**3.5**	**3.2**	**3.2**	**1.5**	**1.5**	**1.4**	**3.4**	**3.7**	**2**

Assume funding for project start begins Oct, 2012 (FY13 funding)

Design and Process Development continues through FY2012

1st complete tile produced Apr, 2014

Summary — STPS Design, Timeline, Infrastructure

- Vacuum transfer system design well-advanced (next presentation by Dean)
  - Costing of major components near complete
  - Complete design still in progress and will be guided by this review
- Required lab infrastructure is being implemented currently
  - Gas lines, compressed air, laminar flow hood, ultrasound cleaner, water purification near complete
  - Electrical service adequate; expect will need work for STPS connections
  - Recirculating chilled water connections available; plumbing throughout labs required
  - Need to address portable cleanroom connected to STPS
- Aim for 1st working sealed tile in 2 years; 1.5 years from funds available

Summary — Processes/Components

- Processes required for Single Tile Process System that are ready to go:
  - Routine production of good quality glass capillary array plates
  - Electroding of MCPs
  - Tile base: sidewall bonded to anode strip bottom plate
  - Grid spacer fabrication
  - Getter holder/spacers
- Processes near-ready:
  - Consistent ALD functionalization of MCPs within target resistance and uniformity
  - Thermopressure indium top seal
- Processes still in development:
  - Photocathode fabrication: uniformity & QE
  - Grid spacer ALD coating: expect minimal challenges
- Untried components/processes:
  - Getter placement, activation, and effectiveness
  - Scrubbing at Argonne: promising results from life tests at SSL